

FIG. 1 is a perspective view of the apparatus of the present invention, showing the base, the support structure, the arm, the gripper, and the end effector.

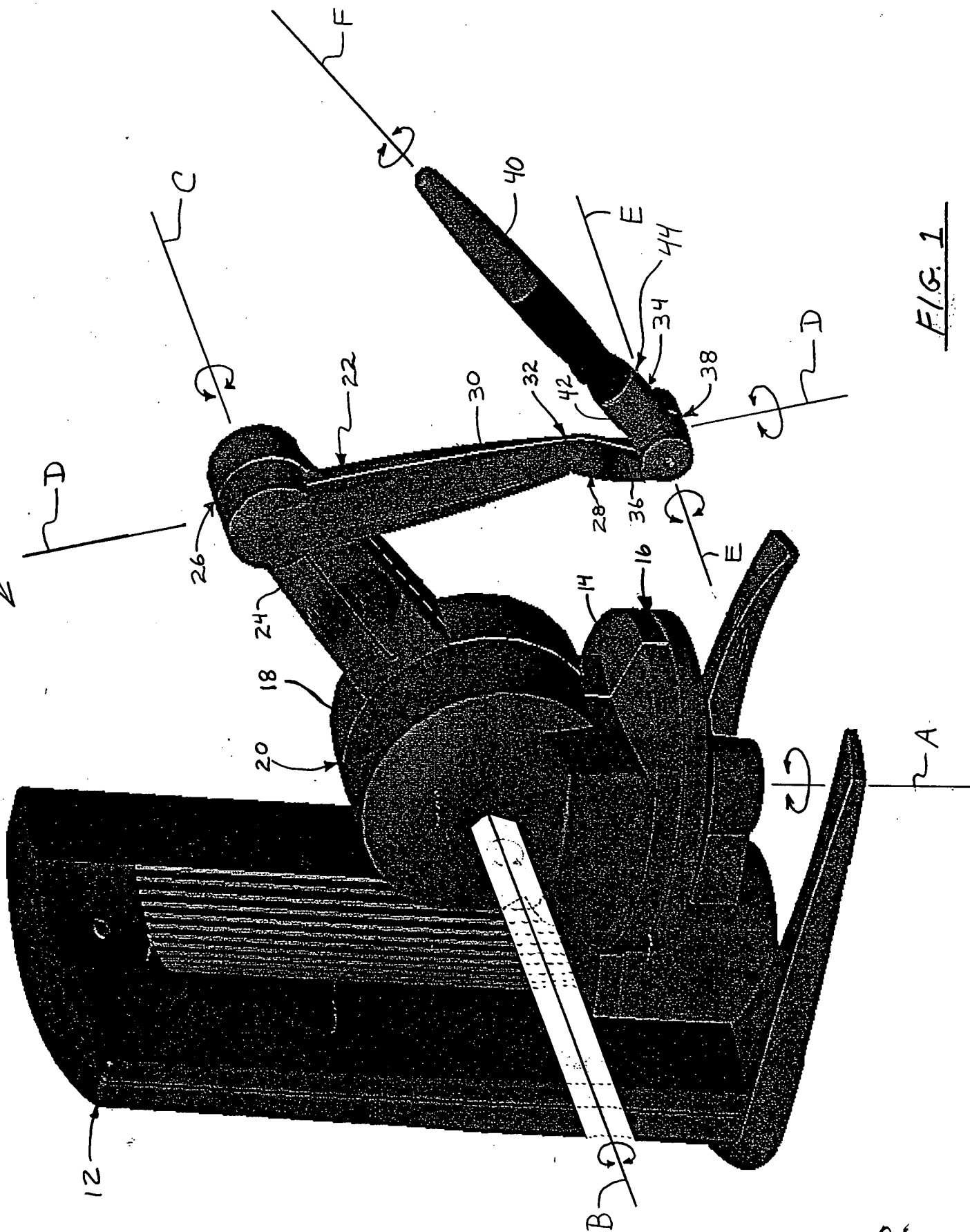


FIG. 1

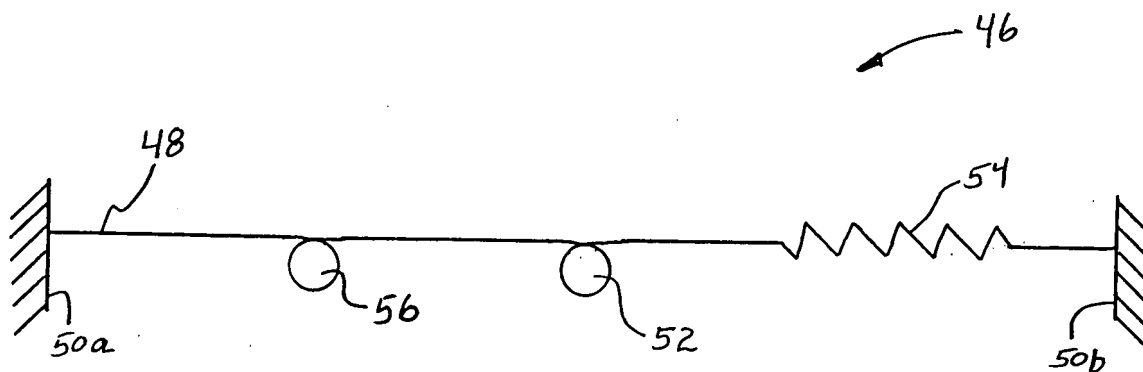


FIG. 2A

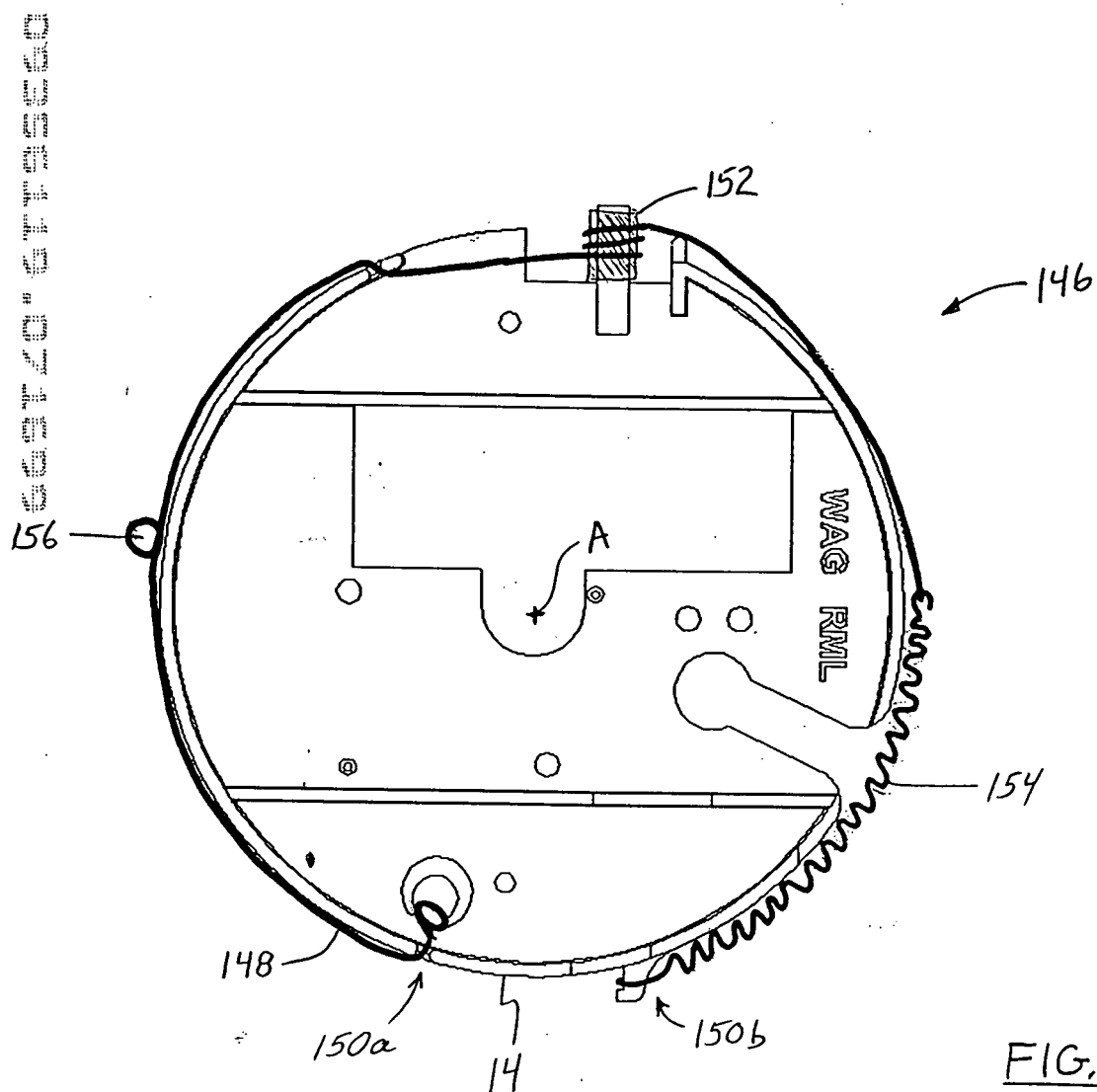


FIG. 2B

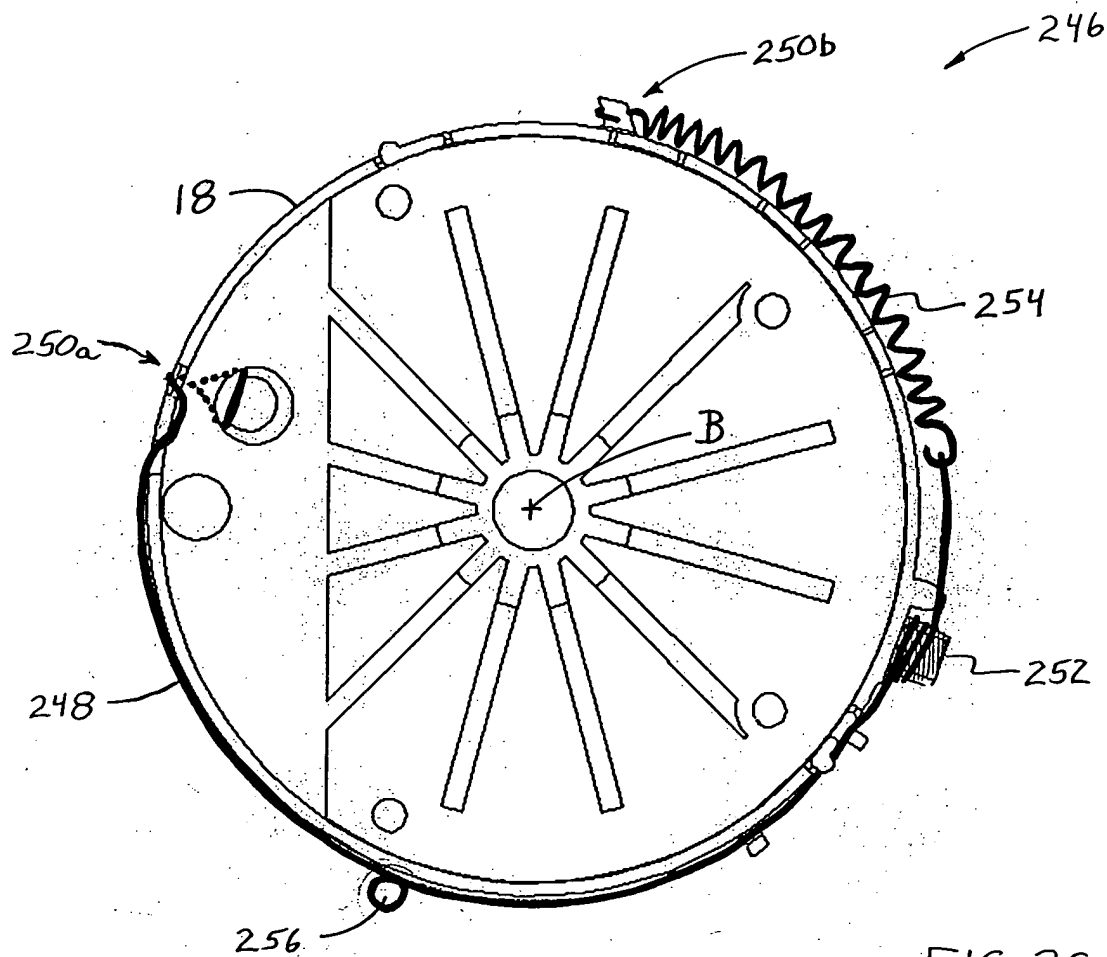


FIG. 2C

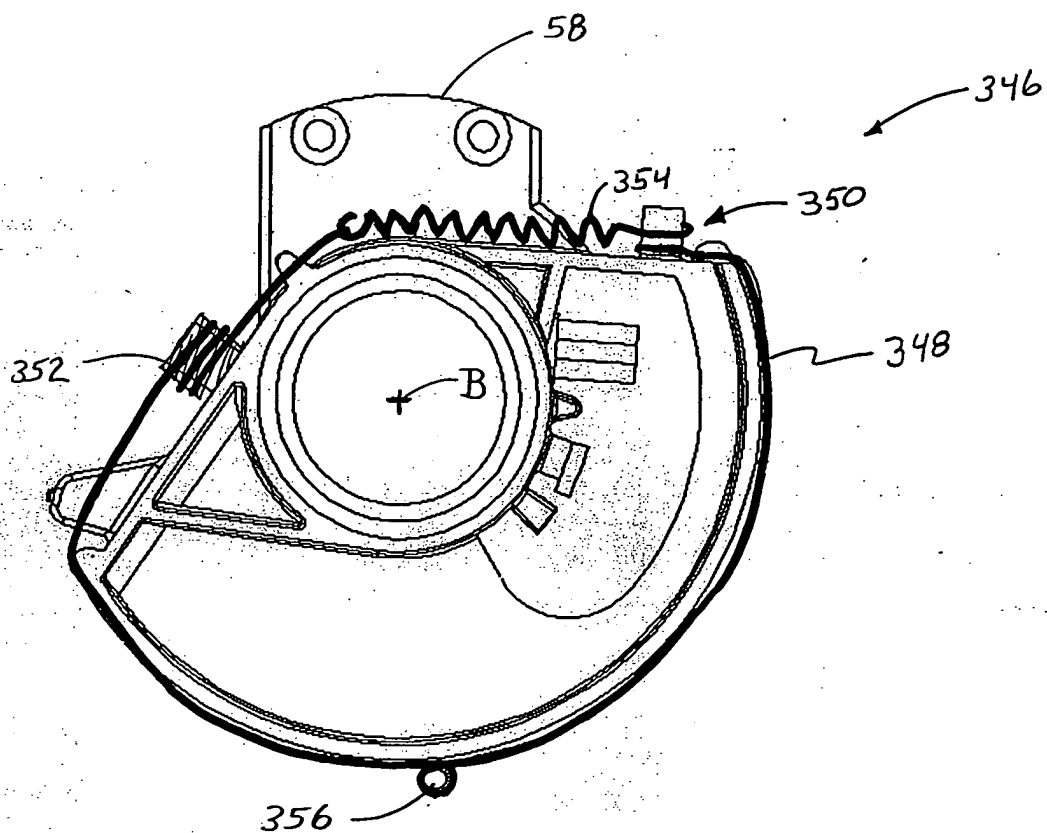


FIG. 2D

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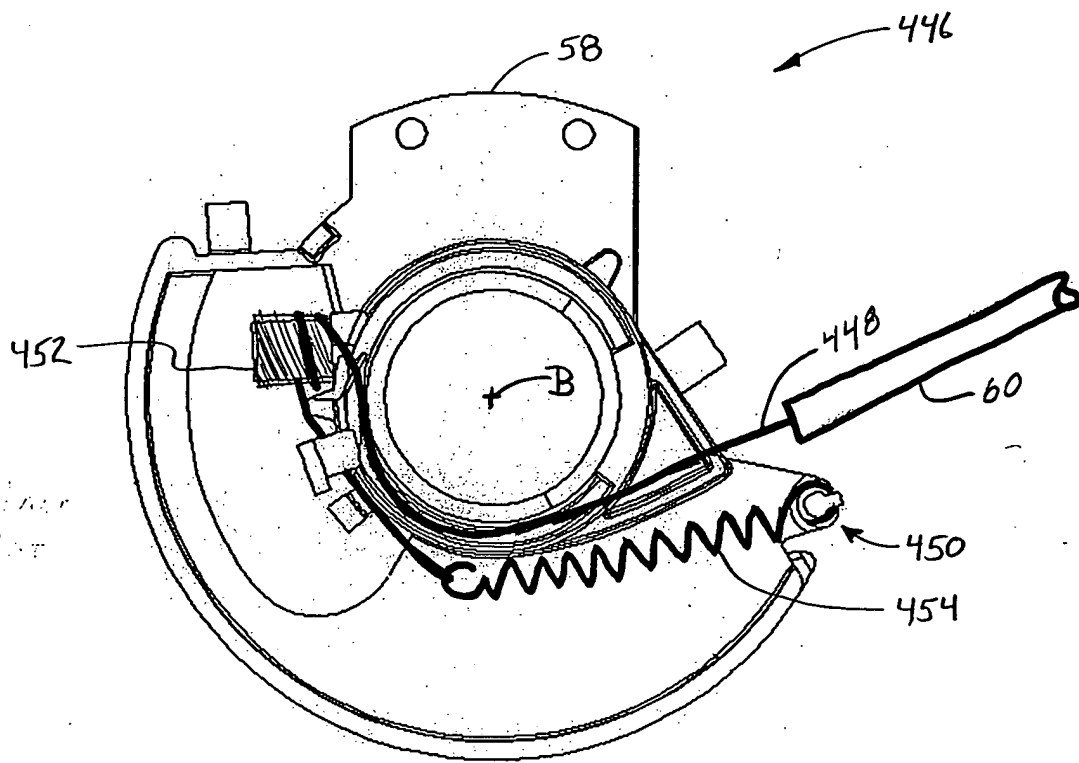


FIG. 2E

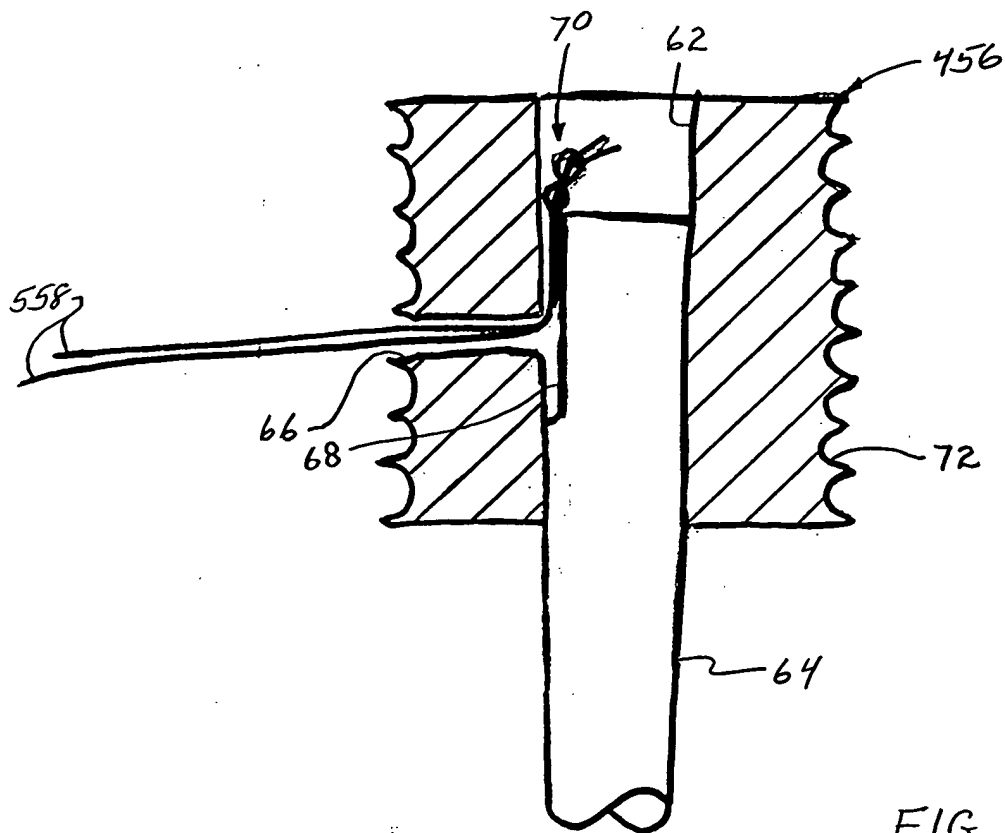


FIG. 3A

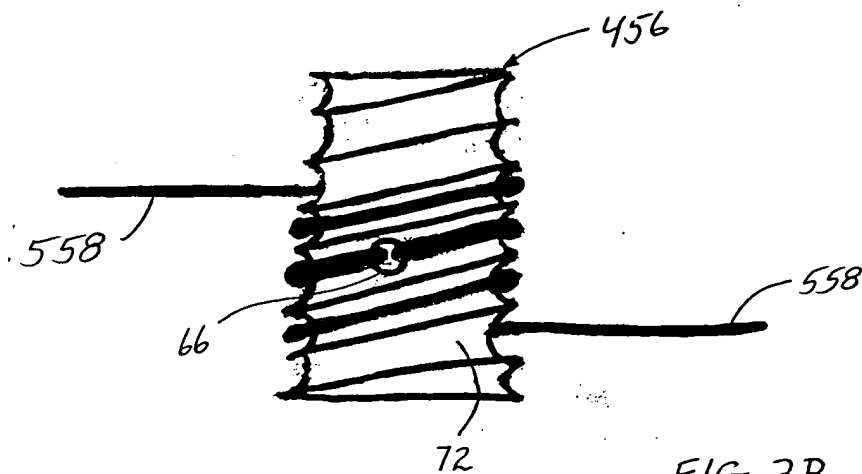


FIG. 3B

FIG. 4A



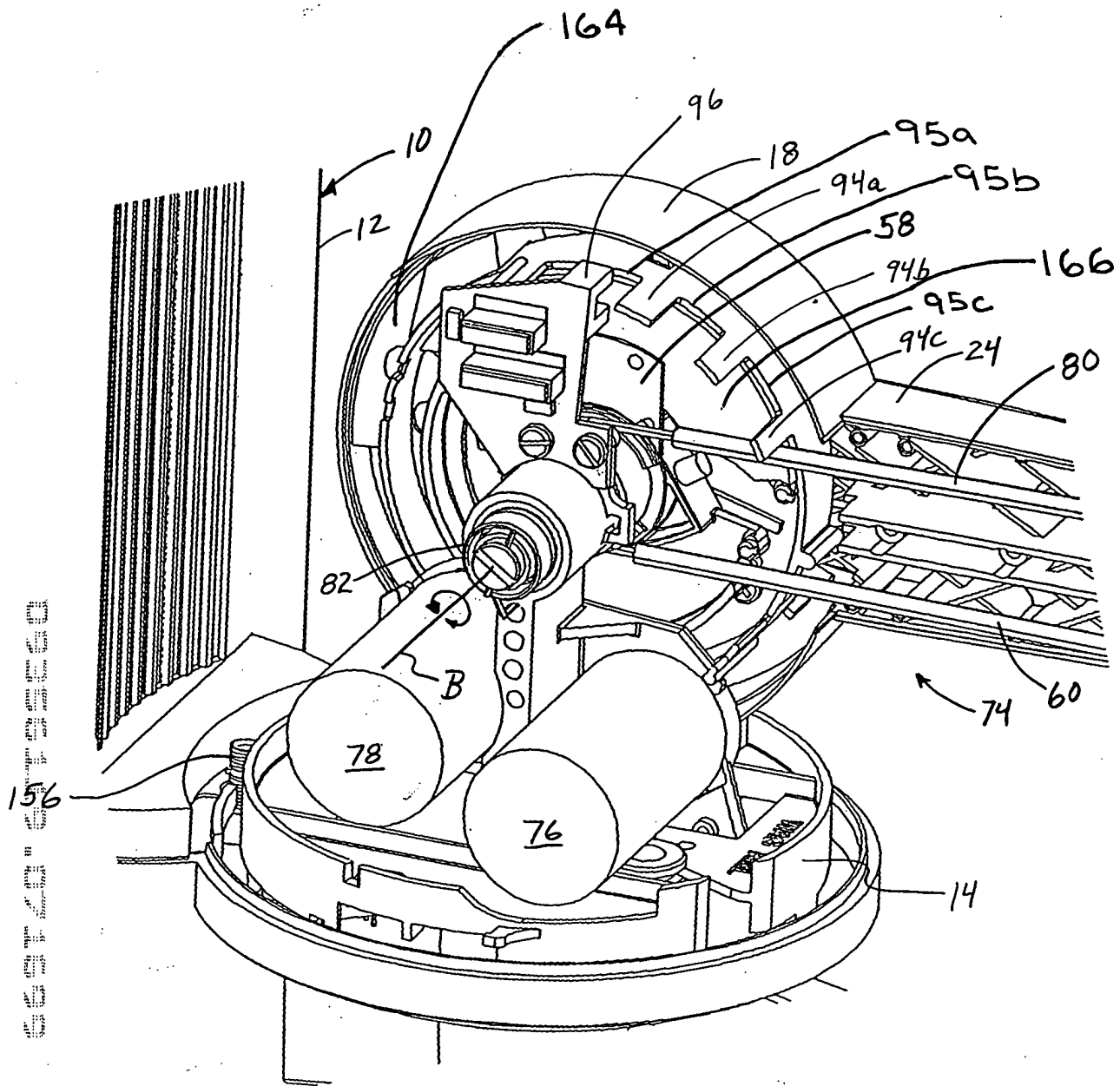


FIG. 4B



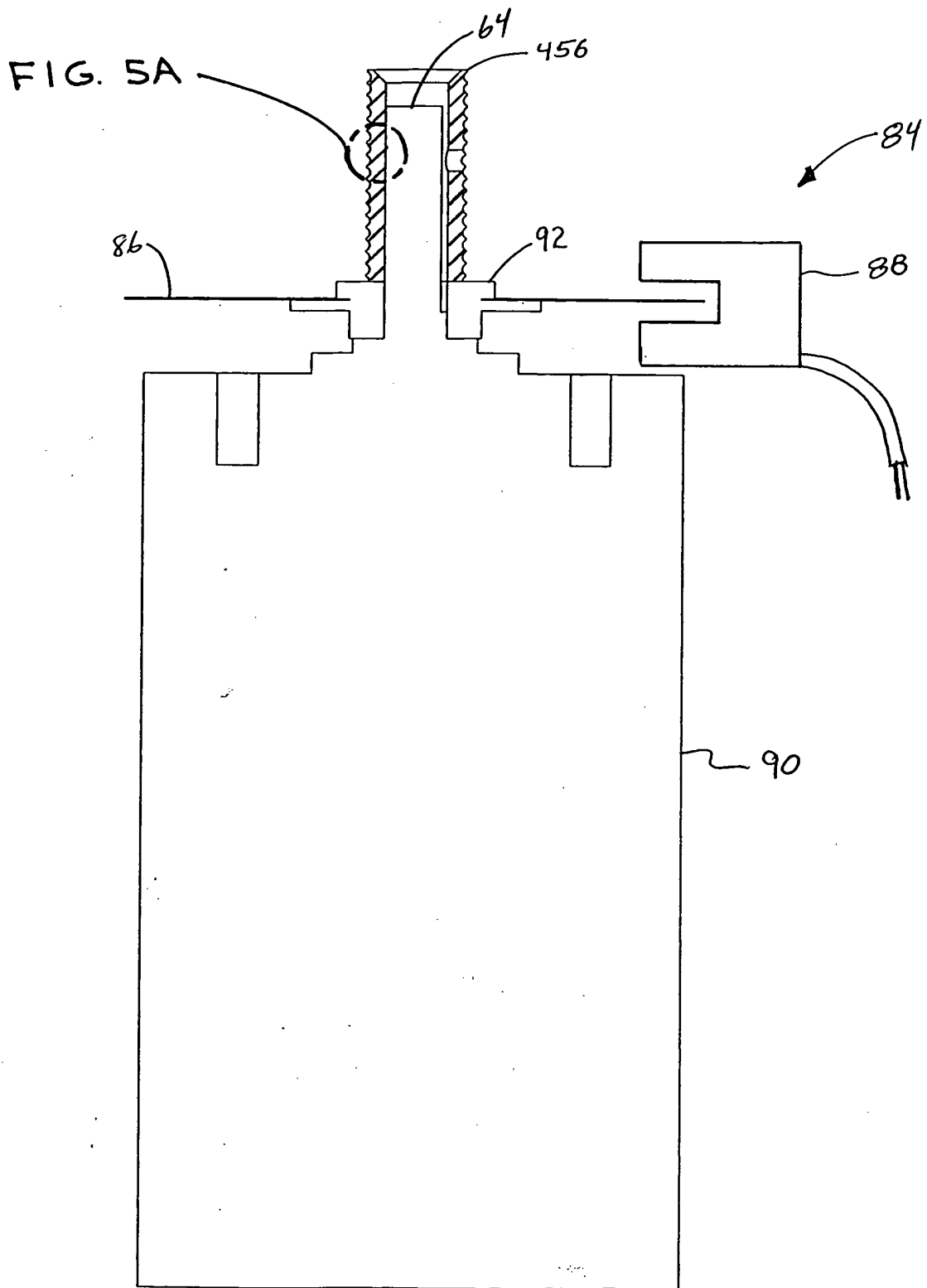


FIG. 5

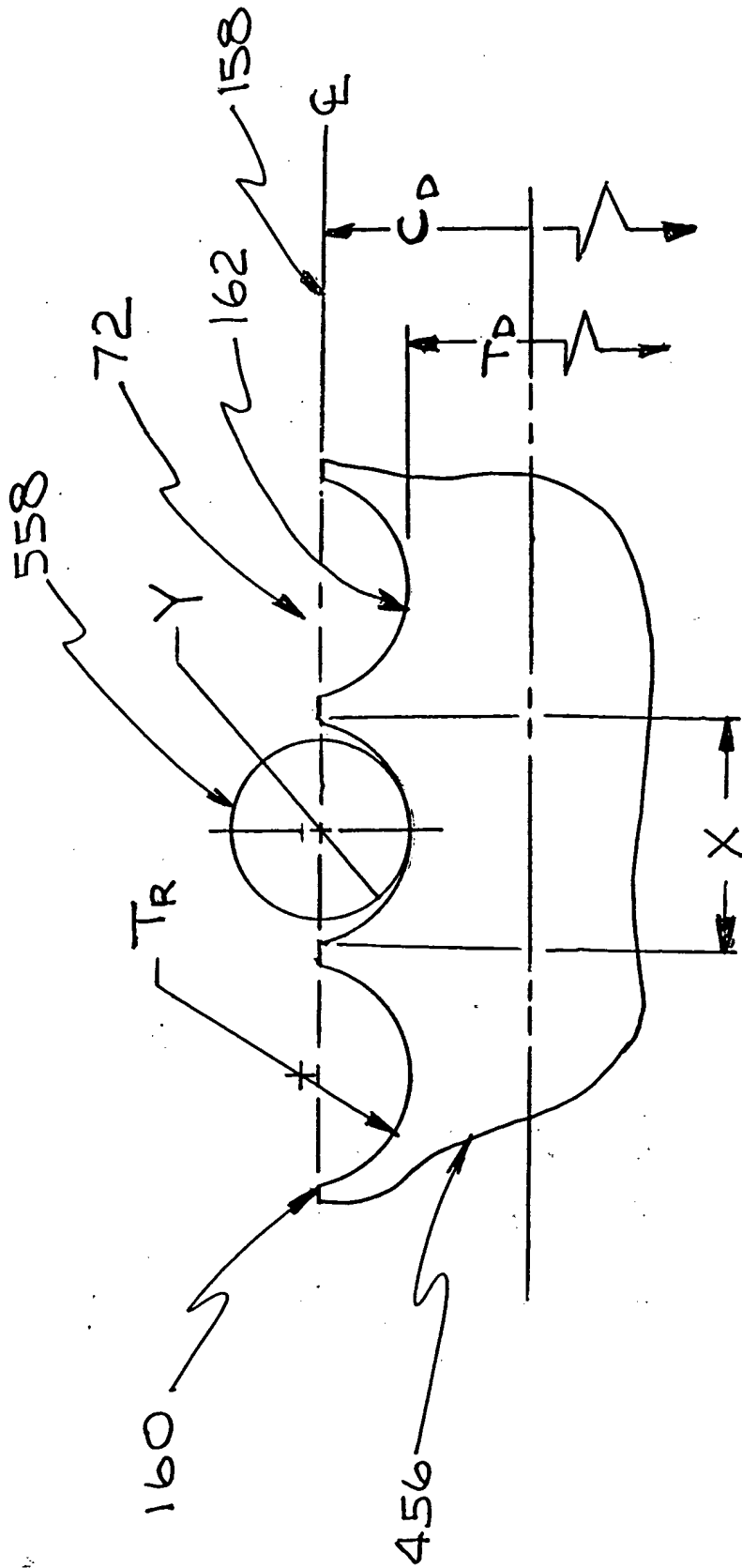


FIG. 5A

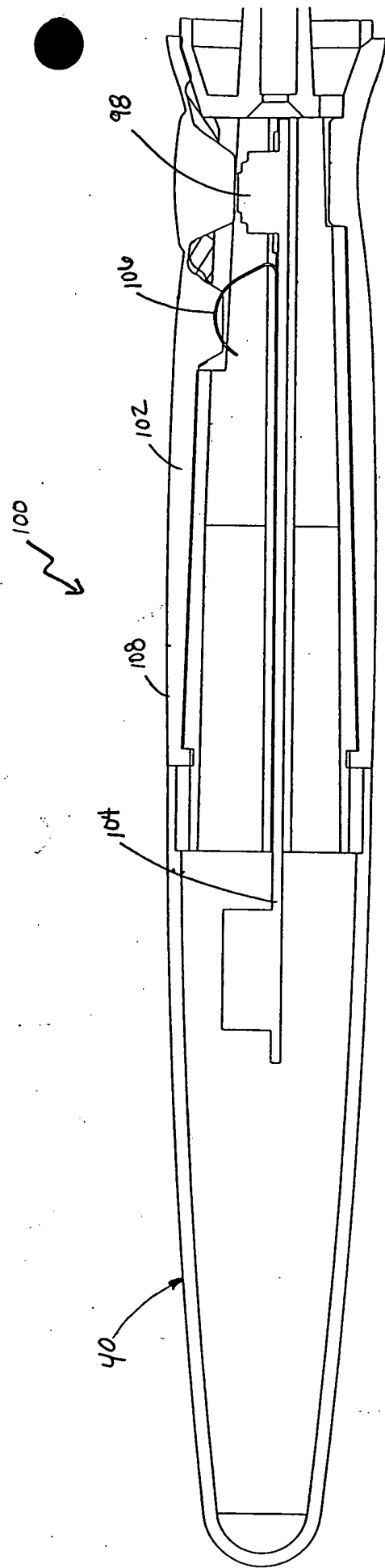


FIG. 6

FIG. 7 is a schematic diagram of a circuit for testing a device under test (DUT) in accordance with the present invention. The circuit includes an oscillator, a signal divider, a variable delay, a phase detector, a pushbutton, and debug LEDs.

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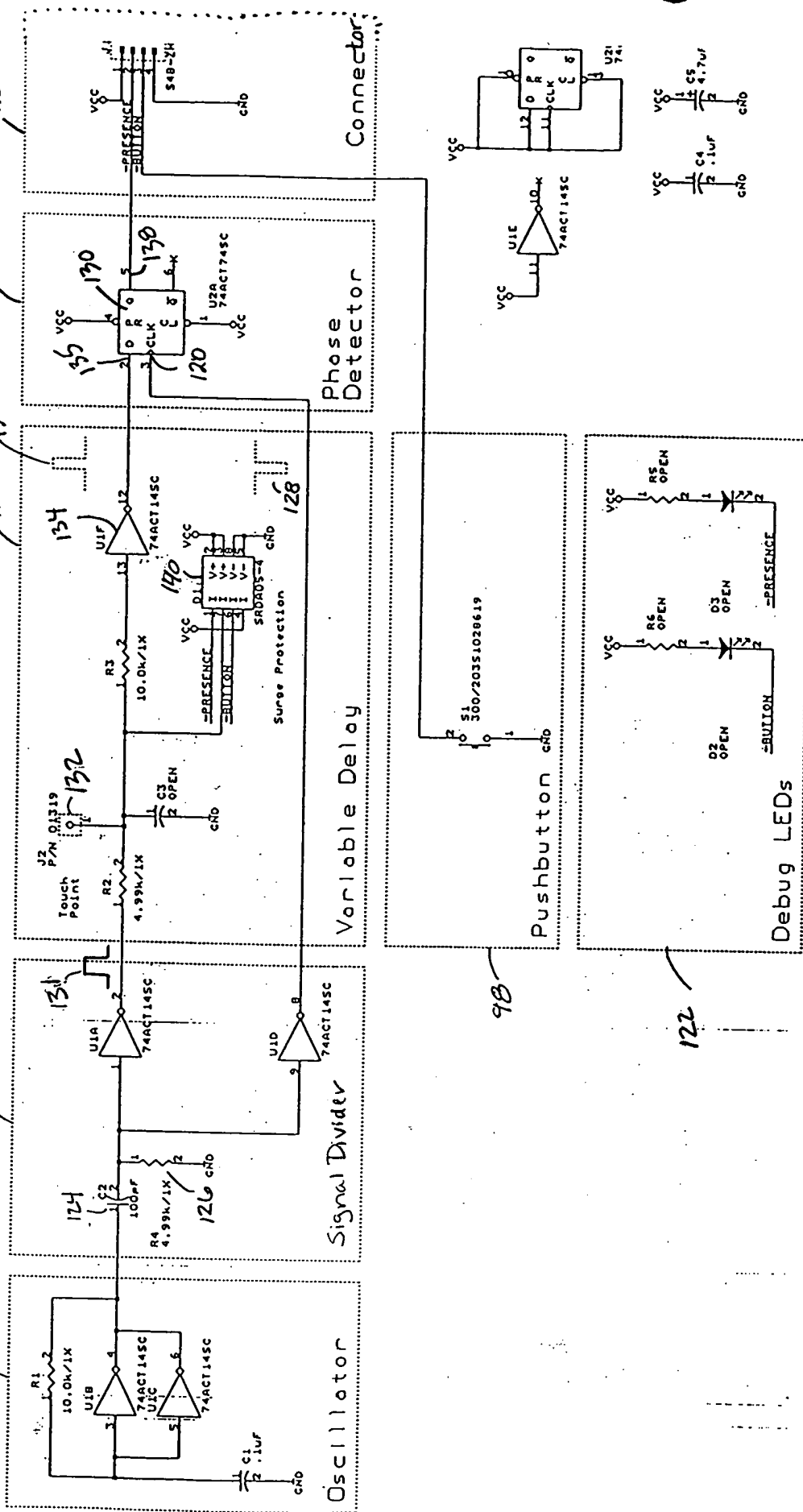


FIG. 7

